Jakub Breier

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Strategic Profile

Hardware Security Researcher with 10+ years of experience in fault injection, side-channel analysis, cryptography, and AI model security. PhD in Information Security and Springer author; active contributor to the hardware security research community with 2,400+ citations and h-index 28. Hands-on expertise spanning cryptographic implementation attacks, physical security of deep learning models, and embedded systems security applied to real-world automotive and industrial hardware. IEEE P3718 Working Group member; CISSP and CACSP certified.

Core Competencies & Technical Expertise

Hardware Security Research: Fault Injection (laser, electromagnetic), Side-Channel Analysis, Physical Security of Deep Learning Models, Hardware Security Modules
Cryptography: Symmetric Ciphers, Post-Quantum Cryptography (Ascon-Sign – NIST PQC Round 1 candidate), Implementation Security, Co-designer of DEFAULT and BAKSHEESH cipher primitives
AI & Machine Learning Security: Physical Attacks on Neural Networks, Fault Backdoor Attacks, Side-Channel Leakage Detection, Adversarial ML Security
Embedded Systems: Automotive ECUs, HMIs, Edge AI Devices, Microcontrollers, FPGAs
Standards & Frameworks: ISO/SAE 21434, IEC 62443, EU Cyber Resilience Act, IEEE P3718[1] (Working Group Member)
Programming & Tools: Python, C/C++, Java, Matlab, Atmel Assembly; Oscilloscopes, Lasers, Pulse Generators, High-Power Amplifiers

Experience

Senior Cyber Security Manager July 2023 - Present
TTControl GmbH *Vienna, Austria*

- Conducted hardware security research on automotive ECUs and HMIs, investigating physical attack surfaces including fault injection and side-channel vulnerabilities on embedded AI and cryptographic implementations
- Contributing researcher on Horizon Europe project aerOS[2], focusing on security of IoT edge-cloud systems
- Founded and operated the company's entire cybersecurity function as the sole security professional, covering 40+ products across automotive ECU and HMI product lines in a 250-person organization
- Delivered end-to-end ISO 21434 CSMS and managed compliance across EU Cyber Resilience Act, IEC 62443, and RED Cyber

Senior Scientist Embedded Security September 2020 – June 2023
Silicon Austria Labs *Graz, Austria*

- Conducted research on physical security of edge AI models, including side-channel vulnerabilities of embedded neural network inference
- Conceived and executed the SECAI project (Security of Edge AI) as sole researcher, from proposal authorship through research delivery
- Published research in IEEE TIFS, TCHES, and other top venues on cryptographic implementation security

Cybersecurity Research Lead / Principal Research Fellow May 2019 – September 2020
HP-NTU Digital Manufacturing Corporate Lab *Singapore*

- Directed a multidisciplinary team of 12 researchers across four industrial projects, managing the full research budget and reporting directly to C-level executives
- Investigated following topics: Secure machine learning; Evaluation of malware detection techniques; 3D object identification; Visual inspection of printed circuit assembly components
- Supported cooperation between the university and HP

Senior Cryptography Security Analyst September 2018 – April 2019
Underwriters Laboratories *Singapore*

[1] https://standards.ieee.org/ieee/3718/12093/
[2] https://aeros-project.eu

- Evaluated security of smart cards against physical attacks and certified them in accordance with certification criteria (EMVco, VISA, MasterCard, American Express)
- Evaluated the resistance of cryptographic implementations used in payment schemes – both public key and symmetric key encryption
- Developed novel attacks and protection methods for side-channel analysis and fault analysis
- Contributed to ISO 17025 certification of the laboratory equipment

Research Scientist (Senior from July 2017) November 2013 – September 2018
Nanyang Technological University *Singapore*

- Unit: Physical Analysis and Cryptographic Engineering Laboratory
- Improved state-of-the-art of secure cryptographic implementations with respect to resistance against physical attacks
- Developed software and hardware countermeasures against side-channel and fault attacks

Visiting Researcher April 2014 – July 2014
Fraunhofer AISEC *Munich, Germany*

- Worked in the field of laser fault injection attacks

Education

Slovak University of Technology Bratislava, Slovakia
PhD in Applied Informatics *25 October 2013*

- Faculty: Faculty of Informatics and Information Technologies
- Thesis title: Security Evaluation Supported by Information Security Risk Mechanisms
- The thesis developed a novel security evaluation with respect to the ISO/IEC 27002 standard and explored new ways of improving the objectivity and the repeatability of such evaluation.

Masaryk University Brno, Czech Republic
Master in Information Technology Security *29 June 2010*

- Faculty: Faculty of Informatics
- Thesis title: Differential Power Analysis of Rijndael Operations on a Selected Microcontroller
- The main goal of the thesis was to perform the differential power analysis attack in different conditions and on multiple implementations of AES.

Slovak University of Technology Bratislava, Slovakia
Bachelor of Informatics *4 July 2008*

- Faculty: Faculty of Informatics and Information Technologies
- Thesis title: Catalogue of Changes Realized by Aspect-oriented Programming
- This thesis aimed to investigate the possibilities of compilation-level changes that could be done by aspect-oriented programming.

Commissions of Trust

- External examiner for Petr Socha's PhD thesis, Prague University of Technology, Czech Republic, 2023
- External examiner for Josef Kokeš's PhD thesis, Prague University of Technology, Czech Republic, 2022
- Reviewer of a grant proposal submitted to the Deutsche Forschungsgemeinschaft (DFG), 2022
- Reviewer of a ViCi grant proposal submitted to The Netherlands Organisation for Scientific Research, NWO, 2019

Editorial Board and Program Committee Memberships (selected venues)

- Editorial board member of the IACR Communications in Cryptology 2024, 2025, 2026
- Hardware and System Security Track Co-chair of the International Symposium on Low Power Electronics and Design (ISLPED) 2025, 2026
- Program committee member of the Hardware Security: Attack and Defense track at The Chips To Systems Conference (DAC) 2026
- Program committee member of the International Symposium on Hardware Oriented Security and Trust (HOST) 2026
- Program committee member of the International Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC) 2022, 2023, 2024, 2025
- Program committee member of the International Workshop on Constructive Side-Channel Analysis and Secure Design (COSADE) 2021, 2022, 2023, 2024

Selected Key Achievements

- Co-designer of *Ascon-Sign*[3], a NIST Post-Quantum Cryptography Competition candidate for Digital Signature Schemes (Round 1 Additional Signatures)
- Co-author of a technical disclosure "Managing Risk when Deploying a Solution Using Machine Learning" in collaboration with Adrian Baldwin and Helen Balinsky from HP Inc.[4]
- Two talks at RSA Conference USA, in 2017 and 2019. RSA Conference is one of the main venues for computer security, hosting around 45,000 participants every year.

Project Participation

- Senior project member for the "Autonomous, Scalable, Trustworthy, Intelligent European Meta Operating System for the IoT Edge-Cloud Continuum" (aerOS) project, funded by the European Commission via Horizon Europe funding programme.
- Project manager and proposal author for the "Security of Edge Artificial Intelligence" (SECAI) project, funded by Silicon Austria Labs, Graz.
- Principal scientist (lead) for four industrial projects in collaboration with HP Inc.: "Secure Machine Learning", "Evaluation of Malware Detection Techniques", "3D Object Identification", and "Visual Inspection of Printed Circuit Assembly Components", co-funded by HP Inc. and National Research Foundation, Singapore.
- Senior project member and proposal co-author for the "Hyper Side-Channel Analysis" (Hyper-SCA) project, funded by DSO National Laboratories, Singapore.
- Senior project member for the "Physical Analysis and Cryptographic Engineering" (PACE) project, funded by DSO National Laboratories, Singapore.

Most Important Scientific Talks

AI-accelerated Implementation Testing: Research vs. Practice
Online; Worcester Polytechnic Institute, WA, USA 10 April 2025

- An Open Source Ecosystem for Implementation Security Testing (OPTIMIST)[5]

Security Evaluation of Vehicular Electronic Control Units
Online; Štrbské Pleso, Slovakia 19 September 2024

- Road Transport Safety Conference BECEP 2024

Hardware Security of Cryptography and Deep Learning
Online; Palo Alto, CA, USA 30 August 2022

[3] https://csrc.nist.gov/csrc/media/Projects/pqc-dig-sig/documents/round-1/spec-files/Ascon-sign-spec-web.pdf
[4] https://www.tdcommons.org/cgi/viewcontent.cgi?article=5267&context=dpubs_series
[5] https://optimist-ose.org/docs/ai/intro

- Dealer Seminar, Palo Alto Research Center (PARC), Xerox

Machine Learning Assisted Differential Distinguishers For Lightweight Ciphers
Online 2 February 2021
- Design, Automation and Test in Europe Conference

Cryptography in Payment Systems
Yogyakarta, Indonesia 26 July 2019
- SEAMS-UGM-ITB Summer Course on Coding Theory and Cryptography

Fully Automated Differential Fault Analysis on Software Implementations of Block Ciphers
Atlanta, USA 28 August 2019
- Conference on Cryptographic Hardware and Embedded Systems

Automated Fault Analysis of Block Cipher Implementations
San Francisco, USA 6 March 2019
- RSA Conference 2019

Fault Analysis Automation on Software Targets
Kharagpur, India 3 July 2018
- Targetted Training on Advanced Side Channel Evaluation of Hardware Security

Fault Injection Attacks and Countermeasures
Brno, Czech Republic 28 March 2018
- Brno Security Meetings, FEKT VUT

Fault Attacks on Cryptographic Devices
Vienna, Austria 18 May 2016
- IEEE CS/SMCS Austria Chapter, SBA Research

Security Evaluation Supported by Information Security Mechanisms
Munich, Germany 25 June 2014
- Technical University Munich, EI SEC PhD Seminar

List of Publications

ORCID: https://orcid.org/0000-0002-7844-5267
Google Scholar: https://scholar.google.com/citations?user=LOENK6IAAAAJ&hl=en
citations: 2430; h-index: 28; i10-index: 60 (as of 23 Mar 2026)

Best paper award:ACM CompSysTech 2012 (conference publication [42])

Preprints & manuscripts under review

[1] Jakub Breier, Štefan Kučerák, and Xiaolu Hou. *The Weight of a Bit: EMFI Sensitivity Analysis of Embedded Deep Learning Models*. Under Review. 2026. URL: https://arxiv.org/abs/2602.16309.

[2] Camilo A Martínez-Mejía, Jesus Solano, Jakub Breier, Dominik Bucko, and Xiaolu Hou. *DeepBaR: Fault backdoor attack on deep neural network layers*. Under Review. 2026. URL: https://arxiv.org/abs/2407.21220.

[3] Ján Mikulec, Jakub Breier, and Xiaolu Hou. *Beyond TVLA: Anderson-Darling Leakage Assessment for Neural Network Side-Channel Leakage Detection*. Under Review. 2026. URL: https://arxiv.org/abs/2603.18647.

[4] Patrik Velčický, Jakub Breier, Mladen Kovačević, and Xiaolu Hou. *DeepNcode: Encoding-Based Protection against Bit-Flip Attacks on Neural Networks*. Under Review. 2026. URL: https://arxiv.org/abs/2405.13891.

[5] Tomáš Gerlich, Jakub Breier, Pavel Sikora, Zdeněk Martinásek, Aron Gohr, Anubhab Baksi, and Xiaolu Hou. *DL-SITM: Deep Learning-based See-in-the-Middle Attack on AES*. Under Review. 2024. URL: https://eprint.iacr.org/2024/1389.

Books

[1] Xiaolu Hou and Jakub Breier. *Cryptography and Embedded Systems Security*. Springer, 2024. ISBN: 978-3-031-62204-5. URL: https://link.springer.com/book/9783031622045.

[2] Jakub Breier, Xiaolu Hou, and Shivam Bhasin. *Automated Methods in Cryptographic Fault Analysis*. Springer, 2019. ISBN: 978-3-030-11333-9. DOI: 10.1007/978-3-030-11333-9.

Book chapters

[1] Jakub Breier. "Foreword". In: *Implementation and Analysis of Ciphers in Quantum Computing*. Ed. by Anubhab Baksi and Kyungbae Jang. Springer, 2023. ISBN: 978-981-97-0024-0. DOI: 10.1007/978-981-97-0025-7.

[2] Lejla Batina, Shivam Bhasin, Jakub Breier, Xiaolu Hou, and Dirmanto Jap. "On Implementation-Level Security of Edge-Based Machine Learning Models". In: *Security and Artificial Intelligence: A Crossdisciplinary Approach*. Ed. by Lejla Batina, Thomas Bäck, Ileana Buhan, and Stjepan Picek. Springer, 2022, pp. 335–359. ISBN: 978-3-030-98795-4. DOI: 10.1007/978-3-030-98795-4_14.

[3] Jakub Breier, Wei He, and Shivam Bhasin. "Reactive Design Strategies Against Fault Injection Attacks". In: *Fault Tolerant Architectures for Cryptography and Hardware Security*. Ed. by Sikhar Patranabis and Debdeep Mukhopadhyay. Singapore: Springer Singapore, 2018, pp. 213–229. ISBN: 978-981-10-1387-4. DOI: 10.1007/978-981-10-1387-4_11.

[4] Jakub Breier, Dirmanto Jap, and Chien-Ning Chen. "Laser-Based Fault Injection on Microcontrollers". In: *Fault Tolerant Architectures for Cryptography and Hardware Security*. Ed. by Sikhar Patranabis and Debdeep Mukhopadhyay. Singapore: Springer Singapore, 2018, pp. 81–110. ISBN: 978-981-10-1387-4. DOI: 10.1007/978-981-10-1387-4_5.

[5] Sikhar Patranabis, Jakub Breier, Debdeep Mukhopadhyay, and Shivam Bhasin. "Side-Channel Assisted Fault Analysis". In: *Fault Tolerant Architectures for Cryptography and Hardware Security*. Ed. by Sikhar Patranabis and Debdeep Mukhopadhyay. Singapore: Springer Singapore, 2018, pp. 59–77. DOI: 10.1007/978-981-10-1387-4_4.

Articles in peer-reviewed journals

[1] Anubhab Baksi, Jakub Breier, Anupam Chattopadhyay, Tomáš Gerlich, Sylvain Guilley, Naina Gupta, Takanori Isobe, Arpan Jati, Petr Jedlicka, Hyunjun Kim, Fukang Liu, Zdeněk Martinásek, Kosei Sakamoto, Hwajeong Seo, and Rentaro Shiba. "BAKSHEESH: Similar Yet Different From GIFT (and ZORRO)". In: *IACR Communications in Cryptology* 2.4 (Jan. 8, 2026). ISSN: 3006-5496. DOI: 10.62056/ae890lmol.

[2] Kyungbae Jang, Anubhab Baksi, Jakub Breier, Hwajeong Seo, and Anupam Chattopadhyay. "Quantum Implementation and Analysis of DEFAULT". In: *Cryptography and Communications* (2025), pp. 359–375. DOI: 10.1007/s12095-023-00666-y.

[3] Leonard Puškáč, Marek Benovič, Jakub Breier, and Xiaolu Hou. "Make Shuffling Great Again: A Side-Channel Resistant Fisher-Yates Algorithm for Protecting Neural Networks". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (2025). DOI: 10.1109/TVLSI.2025.3564357.

[4] Xiaolu Hou, Jakub Breier, and Mladen Kovačević. "Another Look at Side-Channel-Resistant Encoding Schemes". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (2024).

[5] Anubhab Baksi, Shivam Bhasin, Jakub Breier, Dirmanto Jap, and Dhiman Saha. "A Survey on Fault Attacks on Symmetric Key Cryptosystems". In: *ACM Comput. Surv.* 55.4 (2023). ISSN: 0360-0300. DOI: 10.1145/3530054.

[6] Jakub Breier, Xiaolu Hou, Martín Ochoa, and Jesus Solano. "FooBaR: Fault Fooling Backdoor Attack on Neural Network Training". In: *IEEE Transactions on Dependable and Secure Computing* 20.3 (2023), pp. 1895–1908. DOI: 10.1109/TDSC.2022.3166671.

[7] Francesco Berti, Shivam Bhasin, Jakub Breier, Xiaolu Hou, Romain Poussier, François-Xavier Standaert, and Balasz Udvarhelyi. "A Finer-Grain Analysis of the Leakage (Non) Resilience of OCB". In: *IACR Transactions on Cryptographic Hardware and Embedded Systems* (2022), pp. 461–481.

[8] Jakub Breier and Xiaolu Hou. "How Practical Are Fault Injection Attacks, Really?" In: *IEEE Access* 10 (2022), pp. 113122–113130. DOI: 10.1109/ACCESS.2022.3217212.

[9] Jakub Breier, Dirmanto Jap, Xiaolu Hou, Shivam Bhasin, and Yang Liu. "SNIFF: Reverse Engineering of Neural Networks With Fault Attacks". In: *IEEE Transactions on Reliability* 71.4 (2022), pp. 1527–1539. DOI: 10.1109/TR.2021.3105697.

[10] Xiaolu Hou, Jakub Breier, and Shivam Bhasin. "SBCMA: Semi-Blind Combined Middle-Round Attack on Bit-Permutation Ciphers With Application to AEAD Schemes". In: *IEEE Transactions on Information Forensics and Security* 17 (2022), pp. 3677–3690. DOI: 10.1109/TIFS.2022.3213424.

[11] Satyam Kumar, Vishnu Asutosh Dasu, Anubhab Baksi, Santanu Sarkar, Dirmanto Jap, Jakub Breier, and Shivam Bhasin. "Side Channel Attack On Stream Ciphers: A Three-Step Approach To State/Key Recovery". In: *IACR Transactions on Cryptographic Hardware and Embedded Systems* (2022), pp. 166–191.

[12] Xiaolu Hou, Jakub Breier, Dirmanto Jap, Lei Ma, Shivam Bhasin, and Yang Liu. "Physical security of deep learning on edge devices: Comprehensive evaluation of fault injection attack vectors". In: *Microelectronics Reliability* 120 (2021), p. 114116.

[13] Yoo-Seung Won, Xiaolu Hou, Dirmanto Jap, Jakub Breier, and Shivam Bhasin. "Back to the Basics: Seamless Integration of Side-Channel Pre-Processing in Deep Neural Networks". In: *IEEE Transactions on Information Forensics and Security* 16 (2021), pp. 3215–3227.

[14] Manaar Alam, Arnab Bag, Debapriya Basu Roy, Dirmanto Jap, Jakub Breier, Shivam Bhasin, and Debdeep Mukhopadhyay. "Neural Network-based Inherently Fault-tolerant Hardware Cryptographic Primitives without Explicit Redundancy Checks". In: *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 17.1 (2020), pp. 1–30.

[15] Shivam Bhasin, Jakub Breier, Xiaolu Hou, Dirmanto Jap, Romain Poussier, and Siang Meng Sim. "SITM: See-In-The-Middle — Side-Channel Assisted Middle Round Differential Cryptanalysis on SPN Block Ciphers". In: *Transactions on Cryptographic Hardware and Embedded Systems (TCHES)* 3.1 (Nov. 2020), pp. 95–122.

[16] Jakub Breier, Dirmanto Jap, Xiaolu Hou, and Shivam Bhasin. "On Side Channel Vulnerabilities of Bit Permutations in Cryptographic Algorithms". In: *Transactions on Information Forensics and Security (TIFS)* 15 (2020), pp. 1072–1085.

[17] Jakub Breier, Mustafa Khairallah, Xiaolu Hou, and Yang Liu. "A countermeasure against statistical ineffective fault analysis". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 67.12 (2020), pp. 3322–3326.

[18] Jakub Breier, Xiaolu Hou, and Yang Liu. "On evaluating fault resilient encoding schemes in software". In: *IEEE Transactions on Dependable and Secure Computing* (2019).

[19] Xiaolu Hou, Jakub Breier, Fuyuan Zhang, and Liu Yang. "Fully Automated Differential Fault Analysis on Software Implementations of Block Ciphers". In: *Transactions on Cryptographic Hardware and Embedded Systems (TCHES)* 2.3 (May 2019), pp. 1–29.

[20] Sikhar Patranabis, Nilanjan Datta, Dirmanto Jap, Jakub Breier, Shivam Bhasin, and Debdeep Mukhopadhyay. "SCADFA: Combined SCA+DFA Attacks on Block Ciphers with Practical Validations". In: *Transactions on Computers* 68.10 (Oct. 2019), pp. 1498–1510.

[21] Jakub Breier, Xiaolu Hou, and Liu Yang. "Fault Attacks Made Easy: Differential Fault Analysis Automation on Assembly Code". In: *Transactions on Cryptographic Hardware and Embedded Systems (TCHES)* 1.2 (Apr. 2018), pp. 96–122.

[22] Jakub Breier and Jana Branišová. "A Dynamic Rule Creation Based Anomaly Detection Method for Identifying Security Breaches in Log Records". In: *Wireless Personal Communications* 94.3 (2017), pp. 497–511. ISSN: 1572-834X. DOI: 10.1007/s11277-015-3128-1.

[23] Jakub Breier, Wei He, Shivam Bhasin, Dirmanto Jap, Samuel Chef, Hock Guan Ong, and Chee Lip Gan. "Extensive Laser Fault Injection Profiling of 65 nm FPGA". In: *Journal of Hardware and Systems Security* 1.3 (Sept. 2017), pp. 237–251.

[24] Jakub Breier, Wei He, Dirmanto Jap, Shivam Bhasin, and Anupam Chattopadhyay. "Attacks in Reality: The Limits of Concurrent Error Detection Codes against Laser Fault Injection". In: *Journal of Hardware and Systems Security* 1.4 (Dec. 2017), pp. 298–310.

[25] Jakub Breier, Dirmanto Jap, and Shivam Bhasin. "A Study on Analyzing Side-Channel Resistant Encoding Schemes With Respect to Fault Attacks". In: *Journal of Cryptographic Engineering* 7.4 (Nov. 2017), pp. 311–320. ISSN: 2190-8516. DOI: 10.1007/s13389-017-0166-5.

[26] Jakub Breier. "Asset Valuation Method for Dependent Entities". In: *Journal of Internet Services and Information Security* 4.3 (2014), pp. 72–81. ISSN: 2182-2077.

[27] Jakub Breier and Ladislav Hudec. "Security Mechanisms Role in Information Security Evaluation". In: *Information Technology Applications* 1.2 (2012), pp. 5–15. ISSN: 1338-6468.

[28] Jakub Breier and Marcel Kleja. "On Practical Results of the Differential Power Analysis". In: *Journal of Electrical Engineering* 63.2 (2012), pp. 125–129. ISSN: 1335-3632.

International peer-reviewed conferences/proceedings

[1] Zdenko Lehocký, Jakub Breier, Dirmanto Jap, Shivam Bhasin, and Xiaolu Hou. "Side-Channel Analysis of OpenVINO-based Neural Network Models". In: *International Conference on Availability, Reliability and Security (ARES)*. IEEE. 2025.

[2] Aneesh Kandi, Anubhab Baksi, Peizhou Gan, Sylvain Guilley, Tomáš Gerlich, Jakub Breier, Anupam Chattopadhyay, Ritu Ranjan Shrivastwa, Zdeněk Martinásek, and Shivam Bhasin. "Side-Channel and Fault Resistant ASCON Implementation: A Detailed Hardware Evaluation". In: *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE. 2024.

[3] Jan Schröder and Jakub Breier. "RMF: A Risk Measurement Framework for Machine Learning Models". In: *International Conference on Availability, Reliability and Security (ARES)*. IEEE. 2024.

[4] Jakub Breier, Dirmanto Jap, Xiaolu Hou, and Shivam Bhasin. "A Desynchronization-Based Countermeasure Against Side-Channel Analysis of Neural Networks". In: *International Symposium on Cyber Security, Cryptology, and Machine Learning*. Springer. 2023, pp. 296–306.

[5] Anubhab Baksi, Arghya Bhattacharjee, Jakub Breier, Takanori Isobe, and Mridul Nandi. "Big Brother is Watching You: A Closer Look at Backdoor Construction". In: *Security, Privacy, and Applied Cryptography Engineering: 12th International Conference (SPACE'22)*. Jaipur, India: Springer, Dec. 2022, pp. 1–32.

[6] Anubhab Baksi, Shivam Bhasin, Jakub Breier, Anupam Chattopadhyay, and Vinay BY Kumar. "Feeding Three Birds With One Scone: A Generic Duplication Based Countermeasure To Fault Attacks". In: *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2021, pp. 561–564.

[7] Anubhab Baksi, Shivam Bhasin, Jakub Breier, Mustafa Khairallah, Thomas Peyrin, Sumanta Sarkar, and Siang Meng Sim. "DEFAULT: Cipher level resistance against differential fault attack". In: *27th Annual International Conference on the Theory and Application of Cryptology and Information Security (Asiacrypt)*. Springer. 2021.

[8] Anubhab Baksi, Jakub Breier, Yi Chen, and Xiaoyang Dong. "Machine learning assisted differential distinguishers for lightweight ciphers". In: *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2021, pp. 176–181.

[9] Xiaolu Hou, Jakub Breier, and Shivam Bhasin. "DNFA: Differential no-fault analysis of bit permutation based ciphers assisted by side-channel". In: *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2021, pp. 182–187.

[10] Mustafa Khairallah, Xiaolu Hou, Zakaria Najm, Jakub Breier, Shivam Bhasin, and Thomas Peyrin. "SoK : On DFA Vulnerabilities of Substitution-Permutation Networks". In: *2019 ACM SIGSAC Asia Conference on Computer & Communications Security (AsiaCCS)*. Auckland, New Zealand: ACM, 2019, pp. 403–414.

[11] Anubhab Baksi, Shivam Bhasin, Jakub Breier, Mustafa Khairallah, and Thomas Peyrin. "Protecting Block Ciphers against Differential Fault Attacks without Re-keying". In: *2018 IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*. Washington DC, USA, Apr. 2018, pp. 191–194.

[12] Jakub Breier, Xiaolu Hou, Dirmanto Jap, Lei Ma, Shivam Bhasin, and Yang Liu. "Practical Fault Attack on Deep Neural Networks". In: *2018 ACM SIGSAC Conference on Computer & Communications Security (CCS)*. Toronto, Canada: ACM, Oct. 2018, pp. 2204–2206.

[13] Jakub Breier, Dirmanto Jap, and Shivam Bhasin. "SCADPA: Side-Channel Assisted Differential-Plaintext Attack on Bit Permutation Based Ciphers". In: *2018 Design, Automation and Test in Europe (DATE)*. Dresden, Germany: IEEE, Mar. 2018, pp. 1129–1134.

[14] Samuel Chef, Chung Tah Chua, Jing Yun Tay, Yu Wen Siah, Shivam Bhasin, Jakub Breier, and Chee Lip Gan. "Descrambling of Embedded SRAM Using a Laser Probe". In: *2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*. Singapore: IEEE, June 2018, pp. 1–6.

[15] Mustafa Khairallah, Rajat Sadhukhan, Radhamanjari Samanta, Jakub Breier, Shivam Bhasin, Rajat Subhra Chakraborty, Anupam Chattopadhyay, and Debdeep Mukhopadhyay. "DFARPA: Differential Fault Attack Resistant Physical Design Automation". In: *2018 Design, Automation and Test in Europe (DATE)*. Dresden, Germany: IEEE, Mar. 2018, pp. 1171–1174.

[16] Prasanna Ravi, Shivam Bhasin, Jakub Breier, and Anupam Chattopadhyay. "PPAP and iPPAP: PLL-based Protection Against Physical Attacks". In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. Hong Kong SAR, China: IEEE, June 2018, pp. 620–625.

[17] Sayandeep Saha, Dirmanto Jap, Jakub Breier, Shivam Bhasin, Debdeep Mukhopadhyay, and Pallab Dasgupta. "Breaking Redundancy-Based Countermeasures with Random Faults and Power Side Channel". In: *2018 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC)*. Amsterdam, Netherlands: IEEE, Sept. 2018, pp. 1–8.

[18] Jakub Breier, Wei He, and Shivam Bhasin. "An Electromagnetic Fault Injection Sensor using Hogge Phase-Detector". In: *Proceedings of the 18th International Symposium on Quality Electronic Design (ISQED 2017)*. Santa Clara, CA, USA: IEEE, Mar. 2017, pp. 307–312.

[19] Jakub Breier and Xiaolu Hou. "Feeding Two Cats with One Bowl: On Designing a Fault and Side-Channel Resistant Software Encoding Scheme". In: *Topics in Cryptology – CT-RSA 2017: The Cryptographers' Track at the RSA Conference 2017, San Francisco, CA, USA, February 14–17, 2017, Proceedings*. Ed. by Helena Handschuh. Cham: Springer International Publishing, Feb. 2017, pp. 77–94. ISBN: 978-3-319-52153-4. DOI: 10.1007/978-3-319-52153-4_5.

[20] Wei He, Jakub Breier, and Shivam Bhasin. "An FPGA-Compatible PLL-Based Sensor Against Fault Injection Attack". In: *Proceedings of the 22nd Asia and South Pacific Design Automation Conference (ASP-DAC 2017)*. Tokio, Japan, Jan. 2017, pp. 1–2.

[21] S V Dilip Kumar, Sikhar Patranabis, Jakub Breier, Debdeep Mukhopadhyay, Shivam Bhasin, Anupam Chattopadhyay, and Anubhab Baksi. "A Practical Fault Attack on ARX-like Ciphers with a Case Study on ChaCha20". In: *2017 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC)*. Taipei, Taiwan: IEEE, Dec. 2017, pp. 1–8.

[22] Sikhar Patranabis, Debdeep Mukhopadhyay, Jakub Breier, and Shivam Bhasin. "One Plus One is More than Two: A Practical Combination of Power and Fault Analysis Attacks on PRESENT and PRESENT-like Block Ciphers". In: *2017 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC)*. Taipei, Taiwan: IEEE, Dec. 2017, pp. 1–8.

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